Mohit R Khurana

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Awards and Outreach

- Recipient of the prestigious **2025 SME 30 Under 30 Award** from SME org (to be published Oct 2025).
- Recipient of the prestigious **2024 SEMICON West 20 Under 30 Award** from SEMI Americas.
- Honored with over **15 Intel Awards** by substrate, package and wafer assembly TD organizations.
- Committee member of the **IEEE EPS Technical Committee on Emerging Technologies** since 2023.
- Admitted as a **member of The Royal Society of Chemistry** in May 2025.

Experience

- **Intel Corporation - Advanced Design and Customer Enabling, Intel Foundry** Chandler, AZ
  Senior Silicon Packaging Architect - Roadmap and Pathfinding Definition *May 2025 – Present*
  - **Roadmap Definition:** Aligned interconnect and core technology roadmap strategy through analyzing customer demand, market trends and competitive intelligence. Developed and recommended pathfinding strategy to enable a competitive roadmap.
  - **Architecture definition:** Defined architecture and strategy for AI and HPC packaging TV, based on Intel Foundry customer demand and industry trend. Defined considerations for 2.5D and 3D architectures including EMIB 2.5D, Foveros-S 2.5D, Foveros-R/B 2.5D, Foveros-Direct 3D and EMIB 3.5D technologies.
  - **Technology strategy:** Performed trade-off analysis for architecture components including silicon and package size, top fit and layout, technology combos for substrate and power delivery, thermal technologies and system I/O.
  - **Competitive analysis:** Performed competitive analysis and assessment of semiconductor packaging ecosystem including design rules, materials and processes to develop a competitive roadmap.

- **Intel Corporation - Materials TD, Intel Foundry** Chandler, AZ
  Senior Packaging Module Development Engineer - Assembly Materials Integration *Oct 2021 – Apr 2025*
  - **Program management:** Led and qualified assembly materials for next gen packages: wafer assembly (die prep, temporary carrier, epoxy and mold) and package assembly (epoxy underfill, thermals, stiffener, adhesives, passives, BGA) materials.
  - **Product impact:** Successfully qualified materials for Alder Lake (2D FCBGA), Raptor Lake (2D FCBGA), Agliex (EMIB 2.5D), Ponte Vecchio (EMIB 3.5D) products.
  - **EMIB-T package pathfinding:** Led pathfinding and selection of EMIB-T materials, demonstrating successful deployment to pilot line:
    - ▷ Led a cross-platform team of over 8 comprising of materials, process, reliability and mechanical engineers, and integrators defining pathfinding selection and materials strategy.
    - ▷ Selected and qualified new thermo-compression bonding material for EMIB-T die attach via multi-factor DOE, enabling new supplier introduction and achieving yield and reliability targets.
    - ▷ Resolved EMIB-T die bonding issues and defined material property spec based on bump design and bridge die size to establish a technology envelope.
  - **Large form factor warpage strategy:** Led cross-platform team of 6 engineers and roadmap-ed thick stiffener and adhesive materials for large form factor packages (published in Intel's packaging journal):
    - ▷ Defined technology envelope through mechanical modelling, assembly and reliability data on TVs with different form factor, die complex and BGA pitch.

- ▷ Selected stiffener and adhesive material from multiple combinations through multi-factorial DOE, based on technology requirement.
- ▷ Defined design rules to mitigate package warpage and stress for Intel Foundry's AI package roadmap.

◦ **Thermal technology development** Successfully qualified thermal materials and process:

- ▷ Influenced IHS and TIM design to mitigate thermal risks for disaggregated architectures.
- ▷ Optimized IHS flatness, stack-up thickness, process parameters and TIM to meet Rjc targets.

- **Intel Corporation - Yield, Intel Foundry** Chandler, AZ

Packaging Engineer - Platform Lead, Low Yield Analysis *Aug 2019 – Oct 2021*

◦ **Technology Lead:** Led the defect characterization for substrate pathfinding and development for EMIB substrate manufacturing, delivering critical decisions to Department Directors, and Principal Engineers.

◦ **EMIB substrate pathfinding:** Influenced build-up technology selection for EMIB substrate manufacturing for HSIO data center CPUs:

- ▷ Characterized organic adhesive film to elucidate structure-property relationship aimed at improving dielectric-copper adhesion. Published as IEEE ECTC 2022 proceedings.
- ▷ Optimized dielectric lamination, via patterning, copper plating to improve adhesion of a new dielectric material to copper for HSIO enablement.
- ▷ Drove DOEs and characterization methodology to correlate copper roughness to insertion loss.

◦ **Tool procurement:** Led lab characterization tools capability expansion:

- ▷ Negotiated first-of-a kind tool capability development and procurement with tool suppliers.
- ▷ Defined and evaluated multiple tool supplier through a robust sample characterization plan, supplier demo and site visit. Selected and procured tools through data driven decision.
- ▷ Defined purchase specification and completed tool installation and certification for LYA lab.

◦ **Technology innovation:** Demonstrated innovation though novel industry leading technique development (published 2 papers in Intel's packaging journal):

- ▷ Developed nano-mechanical, nano-electrical and nano-chemical AFM methodologies to determine and map localized property delta in modulus, surface potential and functional groups.
- ▷ Developed in-situ heating capabilities for AFM and XRD for packaging applications.
- ▷ Developed automated AFM measurements for packaging, consequently improving lab efficiency.

◦ **Recruitment:** Interviewed and recruited over 10 engineers and technicians resulting in team expansion.

◦ **People management:** Mentored 2 interns guiding them to successful project completions, and multiple engineers on advanced characterization techniques for packaging.

Education

- **Cornell University** Ithaca, NY

Master of Science in Materials Science and Engineering; GPA: ***4.022/4.000*** *Aug. 2017 – Aug. 2019*

- **Institute of Chemical Technology** Mumbai, India

Bachelor of Technology in Polymer Engineering and Technology; GPA: ***8.82/10.00*** *Jul. 2013 – May. 2017*

Skills

Semiconductor Packaging Skills: Flip-chip BGA/LGA, EMIB (2.5D/3.5D), Fan-out RDL and bridge (2.5D), Wafer-level packaging, Silicon interposer (2.5D/3D), SMT, Panel-level substrate.

Process Engineering Skills: FMEA, DOE, SPC, MBPS, Root Cause Analysis, Risk Mitigation, Yield Analysis.

Characterization Skills: Atomic Force Microscopy, XRD, SEM, EDS, FTIR, DSC, TGA, HPLC, GPC, UTM.